APPLICATION NOTE 38

USING THE POWER DESIGN TOOL

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INTRODUCTION

One definition of an oscillator: A circuit with gain and a total phase shift of 360°. Usually 180° comes from the ideal amplifier being inverting. The remaining shift comes from feedback elements and the non-ideal portion of the amplifier.

A second definition of an oscillator: A circuit the power amplifier designer has nightmares about.

If you are looking for a l o n g and b o r i n g Application Note with lots of formulas you no longer remember how to deal with, this is not the document for you. This article works in conjunction with the Apex Power Design CAD tool to remember and apply correctly all the rules and formulas, thus allowing concentration on the big picture. As a toddler, you probably had toys that gave you the "feel" that square pegs do not fit in round holes. The objective here is to give you a "feel" for what curve to bend in which direction allowing you to slay the evil dragon of power amplifiers, the oscillator.

WHY THE DRAGON APPEARS

By far and away, the most common cause of oscillation is lack of adequate supply bypassing! This is often true even of circuits having hundreds or even thousands of microfarads of bypass. It is all too easy to forget details such as:

1. The amplifier has gain into the MHz range even when used at DC.
2. In the MHz range, some capacitors have significant inductive reactance.
3. Even a straight piece of wire has inductance.
4. Resistance of PC traces and even wire makes a difference in power circuits.

Bypassing supplies for a power amplifier is such a broadband job that it often requires multiple sets of components and demands proper placement of each set. For the high frequency spectrum (this includes the frequency where the amplifier runs out of gain) the use of small value ceramic capacitors placed right at the pins of the amplifier is required. In the range of the signal frequency, capacitors will be larger in value and physical size so they will be further from the supply pins of the amplifier. Relying on the output capacitors of the power supply may be acceptable, but not if they are multiple feet from the amplifier.

The second most common cause of oscillation is the elusive ground loop. Refer to Figure 1 for an over-simplified picture of the problem. Load currents flowing through the parasitic impedances in the line back to the supply, develop voltages which are inserted as positive feedback. To break the loop, designate one physical point as the center of a star ground. Make sure every connection to ground has its own path to the center of the star. Do not forget the low side of the bypass capacitors. The best news about this problem is that the frequency of oscillation usually points to the cause by being right at the unity gain frequency of the amplifier.

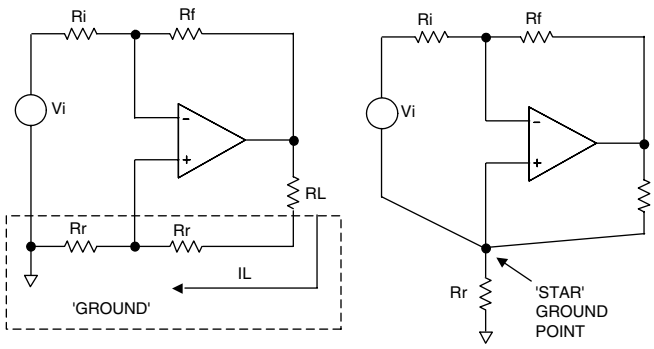


FIGURE 1. GROUND LOOPS AND THEIR SOLUTIONS SIMPLIFIED

The least common cause of oscillation is related to design of the output stage of the amplifier itself and also raises a flag to identify itself. If the oscillation is above the unity gain frequency of the overall amplifier (below 0db on the bode plot), we have a local feedback problem in the output stage. First, check supply bypass. Then try a snubber network (series R-C connected from the output to ground) in the range of 1 to 10 ohms and 0.1 to 1uF.

What about exceeding the capacitive load specification that appears on most op amp data sheets? This refers to Cload with the amplifier connected in a unity gain configuration. We will examine means to circumvent this limitation.

THE GROUND RULES DEFINING THE PLAYING FIELD

With the above out of the way, we can attack the real subject of this article-taming oscillations caused by the non-ideal characteristics of the amplifier and feedback elements. A few more definitions are in order:

Closed loop response is the relationship between the input and output signals of the total amplifier (including feedback). We will be looking at both the gain and the phase of this response.

Open loop response is the relationship between the input and output signals of the amplifier without feedback. This response does not go away when we close the loop. It is still the input to output pin relationship and it does affect closed loop response.

Loop gain is the difference between the open and closed loop gains. This is the magic of op amps allowing overall circuit function to be primarily a function of feedback elements. It allows an op amp to be a general purpose building block. More loop gain means the circuit will be more faithful to the ideal closed loop response.

Beta is the fraction of the output signal fed back to the negative input of the op amp. We refer more often to the reciprocal which is closely related to inverting signal gain. It is imperative to note that stability analysis is treated as a non-inverting circuit, just as when calculating the effects of voltage offset on the output signal. This means gain, or 1/beta can never go below one or 0db.

Intersection rate is the slope difference between the open and closed loop roll-off at the point where they cross.

Closure frequency is the frequency where open loop gain is 0db. Above this frequency the circuit can not meet the definition of an oscillator.

Phase margin is the difference between the 360°of the oscillator definition and the phase shift of the total circuit at closure frequency. In practical circuits, it is recommended that all frequencies below closure be examined as well. Note also that by using negative feedback to close the loop we have the

first 180° of phase shift needed to oscillate simply from the inverting function of the op amp. The phase plots you will see do not reflect the inversion, only the change over frequency. This further means that on all the phase plots to follow, phase margin will be the difference between the curve and 180°.

Phase margin is the buffer zone between the power amplifier and the power oscillator. 45° is desirable, more is better, never accept less than 30.

Straight line approximation is the technique used to plot most of the response curves to follow. While real performance would be represented by smooth curves, the straight segments make it much easier to pinpoint corner frequencies. The penalty in terms of phase accuracy is +/-6°.

SNAP SHOT OF A CLASSIC AMPLIFIER POWER DESIGN MECHANICS

The data entry screen of the Cload sheet is shown in Figure 2. Yellow cells are for data entry and their labels correspond to component labels of the schematic. Entering actual, extremely high or zero values can model the most common stabilization techniques. Comment cells will instruct you how to enter data for your own operational amplifier, but Apex hopes you will use the pull down to select one of theirs from the built-in data base. The first thing Power Design should be able to do is duplicate the small signal response (or bode plot) and the open loop phase response of the given amplifier.

For amplifier models featuring external compensation, Power Design uses a three digit suffix to specify compensation capacitor values detailed on the product data sheet. The Rcl entry allows entry of the current limit setting used with most power amplifiers. Enter the remaining circuit values according to your application. Setting up the PA85 (compensated for unity gain) as a unity gain buffer (Rin=very high, Rf=very low) will produce the graphs shown in Figure 3. Open loop response should duplicate what is shown in the data sheet, or measured values of your own amplifier.

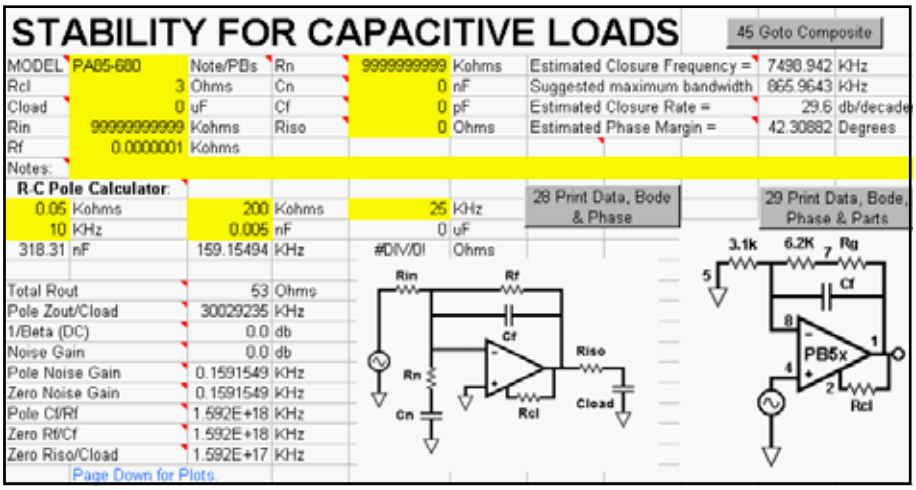


FIGURE 2. DATA ENTRY FOR CLOAD ANALYSIS

The data entry screen of the Cload sheet is shown in Figure 2. Yellow cells are for data entry and their labels correspond to component labels of the schematic. Entering actual, extremely high or zero values can model the most common stabilization techniques. Comment cells will instruct you how to enter data for your own operational amplifier, but Apex hopes you will use the pull down to select one of theirs from the built-in data base. The first thing Power Design should be able to do is duplicate the small signal response (or bode plot) and the open loop phase response of the given amplifier.

In the upper right corner of Figure 2, are some answers that illustrate what this whole exercise is about. The most important answer is phase margin where we like to see 45°. Closure

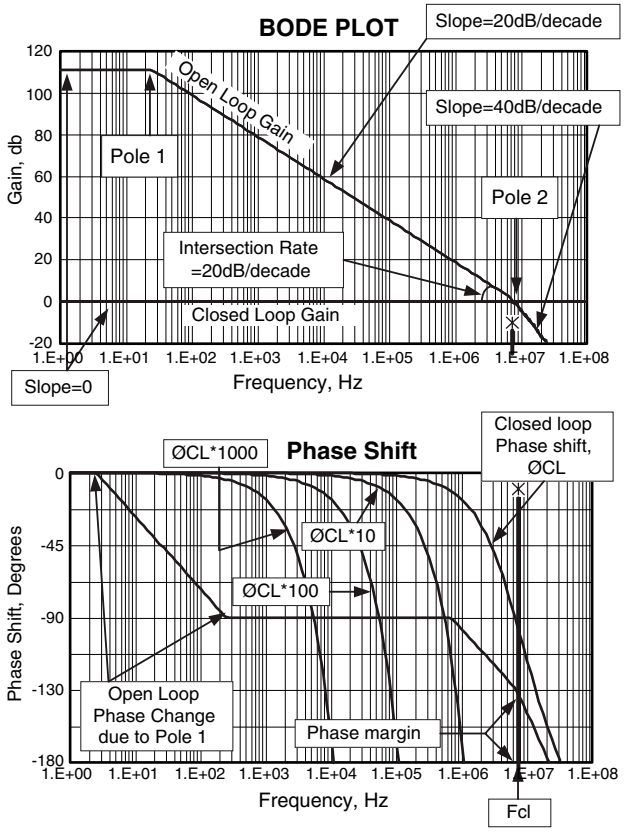


FIGURE 3. UNITY GAIN STABLE AMPLIFIER CURVES

(intersection) rate is a key indicator of health, where 20 is the desired number. The number is usually a multiple of 20 but as you see here, when the intersection and a corner frequency are nearly coincident, it may fall in between. The suggested maximum bandwidth is the frequency where loop gain is down to 20db. This is very much a judgement call and will be application dependent. Remember the basic op amp theory where various internal errors are reduced by the loop gain when the circuit is closed. For example, open loop output impedance (affecting gain accuracy) of 10 ohms would be a killer with a 1A output. If the circuit has 40db of loop gain, this error drops from 10V to 0.1V. Demanding this 40db would reduce the suggested maximum bandwidth by a decade.

The unity gain stable op amp will have its first pole at a low frequency and the second pole will not appear until open loop gain has crossed 0db. The horizontal line at 0db indicates closed loop unity gain operation. Notice that pole 1 of the open loop response is at roughly 25Hz, that phase started moving a decade before this and within 2 decades has moved 90*. We find the second pole at about 7MHz and again phase starts moving a decade before. While the third pole does not show on the bode plot, a corner in the phase plot around 7MHz tells us pole 3 is near 70MHz. The main point of interest for stability concerns is at Fcl where intersection rate is 20db per decade and open loop phase is about 135°. This means the phase margin is about 45°.

The R-C Pole Calculator is a convenience item having no effect on any of the results. However, it does make it easy to translate graphic data to component values. Below this are listed many of the operating points of the circuit. As experience is gained using this tool, you will start using some of these numbers directly to eliminate paging down to the graphs.

In contrast, Figure 4 shows the same amplifier compensated for a gain of 100, but still configured for unity gain. Pole 1 has moved up in frequency giving us a greater gain-bandwidth product, but notice that pole 2 is now well above 0db and the intersection rate is 40db per decade. Our phase margin has disappeared. This example is a little radical, but it does show the dangers of improper compensation. There are also some op amps having a minimum gain specification which would fit this same general picture if used below the minimum gain spec.

In the following examples, we will first attempt to obtain an intersection rate of 20db per decade (a very good sign but not a guarantee) by visualizing line segments and then checking out the actual phase graph.

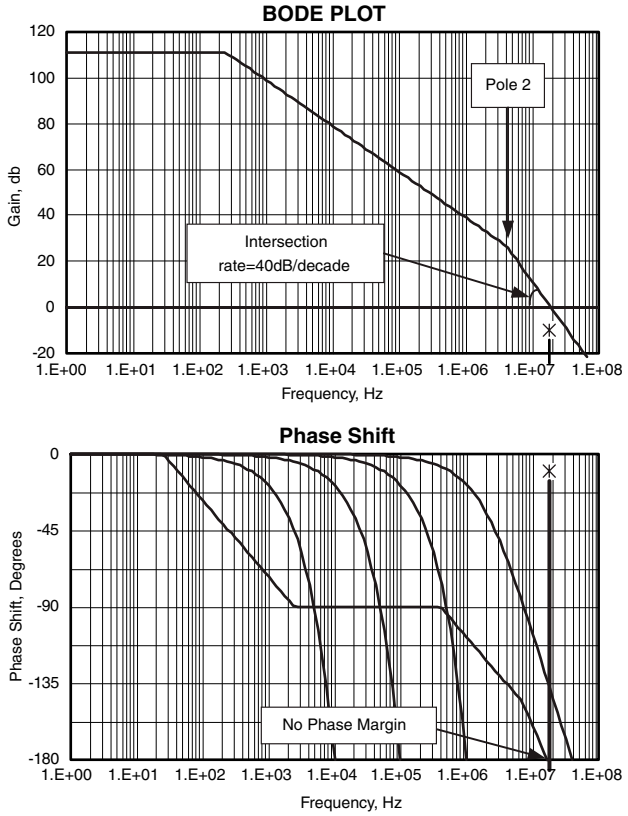


FIGURE 4. ATTEMPTING TO USE AN AMPLIFIER BELOW SPECIFIED MINIMUM GAIN

LARGE CAPACITIVE LOADS CAUSE PROBLEMS

Open loop output impedance of an amplifier forms a pole with a capacitive load, which is modeled as an additional pole in the small signal response as shown in Figure 5. This is our same amplifier (compensation recommended for gain=20), attempting to drive a heavy Cload with an inverting gain of 19. Note that this pole introduced with the addition of an external component is causing the same 90° shift of phase; 45° taking place below the pole frequency and the other half above. Any time the combination of Zout (sum of the amplifier output impedance and any other resistance inside the loop) and Cload is large enough to place this pole below closure frequency. The intersection rate will no longer be 20db per decade and stability will be in question.

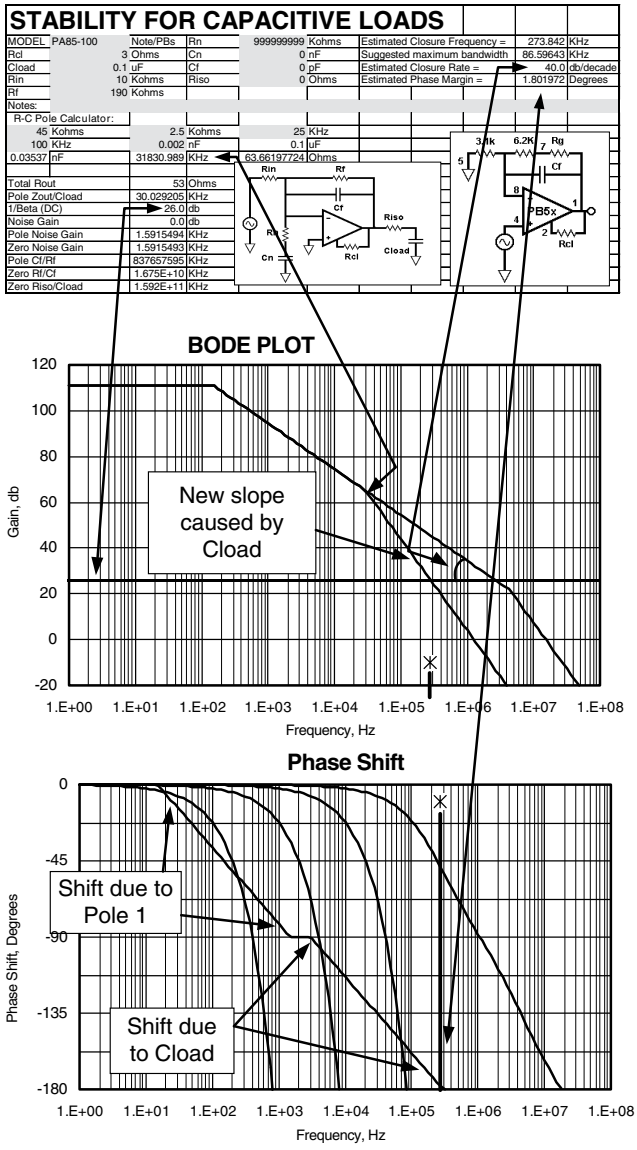


FIGURE 5. MODELING A LARGE CAPACITIVE LOAD

It is now time to start the process of visualizing potential solutions. We know good intersection rate is a key. Sometimes we can change amplifier compensation to move the open loop response, but usually not enough to cure this problem. One thing we might do is increase the closed loop gain to 66db. Entering Rin=.1 results in the data shown in Figure 6 (next page) where the stability problem now looks fine with a phase margin of ~45°. There are several problems associated with this solution. The most obvious is that we have changed the closed loop transfer function which now requires other system changes to compensate. Next, DC errors due to voltage offset and drift are up by a factor of 100! Also notice that if we demand the recommended 20db of loop gain, circuit bandwidth is only ~2.7KHz, about a factor of 30 reduction. This solution is rarely acceptable.

USING AN ISOLATION RESISTOR

Go back to Figure 5 and imagine we have the power to grab the segment modeling the effect of our Cload, just above the intersection point (about 200KHz & 30db) and bend it back to a minus 20db/decade slope. This would result in a new intersection rate of 20db/decade. This is exactly what an isolation resistor does for us! The R-C Pole calculator is pre-loaded

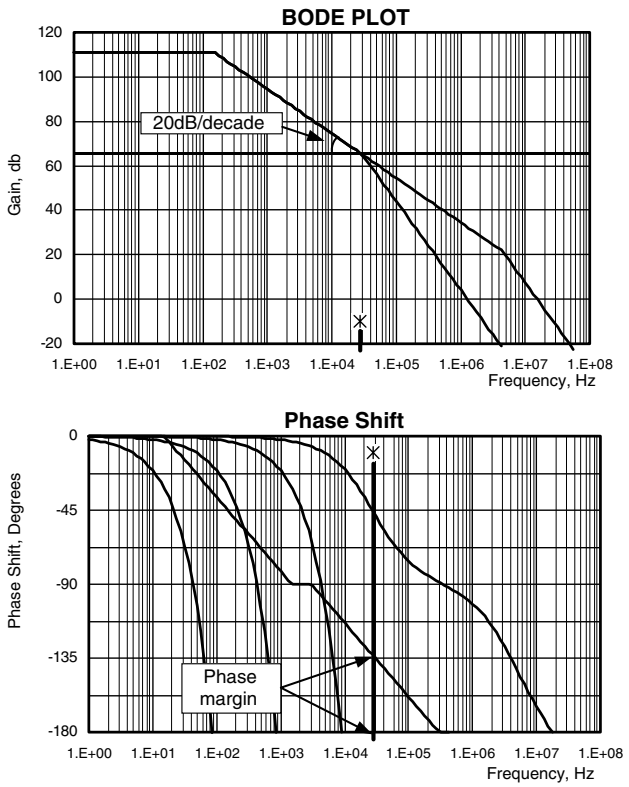


FIGURE 6. INCREASED GAIN YIELDS ACCEPTABLE PHASE MARGIN

with the Cload value and prescribes 8 ohms when we enter the corner frequency of 200KHz. Figure 7 shows the results of entering 8.2 ohms as Riso.

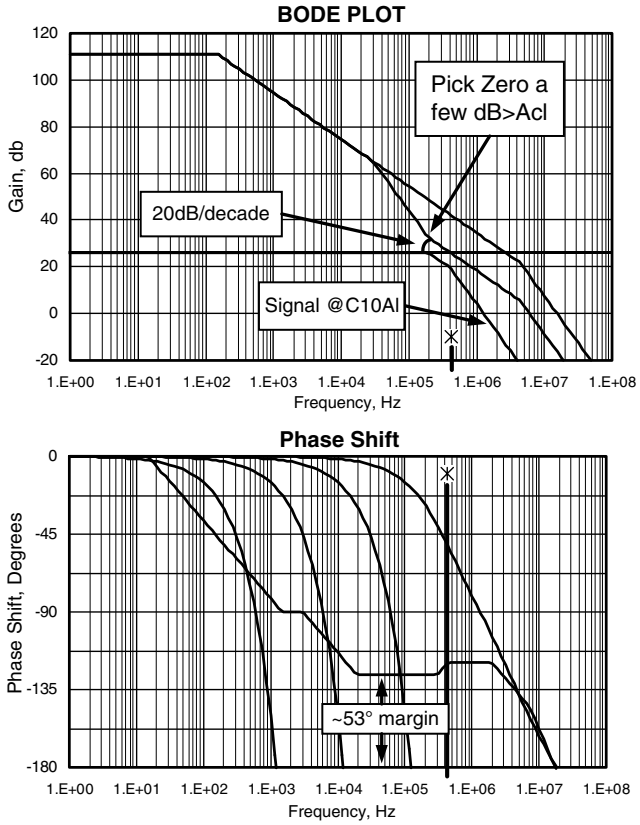


FIGURE 7. AN ISOLATION RESISTOR IS OFTEN THE BEST STABILIZATION METHOD

What about larger values of Riso? They will produce stable circuits but there are two things you need to know. Riso is outside the feedback loop where voltage drops and phase shifts are not corrected by loop gain. The curve labeled "Signal at Cload" shows roll off of the signal at the actual load. Check Figure 8 to see the effect of increasing Riso to 40 ohms. The load is now rolled off at 40KHz cutting usable bandwidth to about half that of the 8.2 ohm solution. The suggested maximum bandwidth cell does not take this into account. Also, phase shift outside the loop is not reported by Power Design.

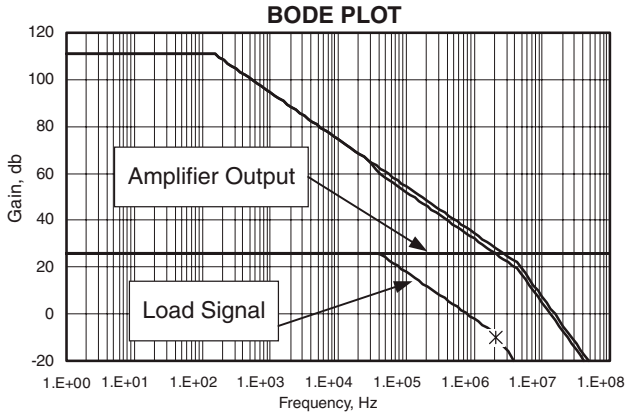


FIGURE 8. THE BANDWIDTH PENALTY IMPOSED BY LARGE ISOLATION RESISTORS

Do not let these drawbacks to the isolation resistor technique scare you off. It is the easest to visualize from the graph; generally not bothered by parasitics; works equally well for inverting and non-inverting circuits; and it is very tolerant of variations in Cload. This circuit remains stable even if the load capacitance increases several orders of magnitude. This is true because the singular value of Cload forms both a pole with the amplifier output impedance and a zero with Riso. These tend to cancel each other as they move up and down the frequency spectrum together with changes in Cload. Obviously, huge values of capacitance reduce bandwidth.

THE ROLL OFF CAPACITOR

We know a capacitor across the feedback resistor will attenuate high frequency gain or roll off the circuit, changing slope of the closed loop gain from zero to -20db/decade. If we position the pole of this roll off correctly, it will cross the open loop gain curve producing an intersection rate of 20db/decade giving a good shot at stability. We also know that 1/beta is the critical factor in stability analysis; it must be thought of as non-inverting; and non-inverting gain (or 1/beta) can never go below 0db. This means the desired segment of 1/beta will have a -20db/decade slope, starting at 26db and stopping at 0db. Here's where the vision or feel of things comes in. Look again at the graph of Figure 5, our problem statement. Picture (maybe with the help of a straight edge) a line segment with a -20db/decade slope crossing the open loop gain curve at half the closed loop gain (13db in this case). At what frequency will this segment cross the closed loop gain (26db)? With a little practice, your vision will yield about 150KHz and the R-C Pole Calculator will tell you 5.6pF across the 190K ohms is the place to be. See Figure 9 (next page) for the results.

We now have a paper circuit with ~54° phase margin, the desired gain, acceptable DC accuracy and a recommended bandwidth of 86KHz. The reason for the phrase "paper circuit" has to do with parasitic capacitance, which can vary wildly with quality of the physical layout. If the actual layout were to add 5pF to the feedback capacitor, we would loose almost 20° of

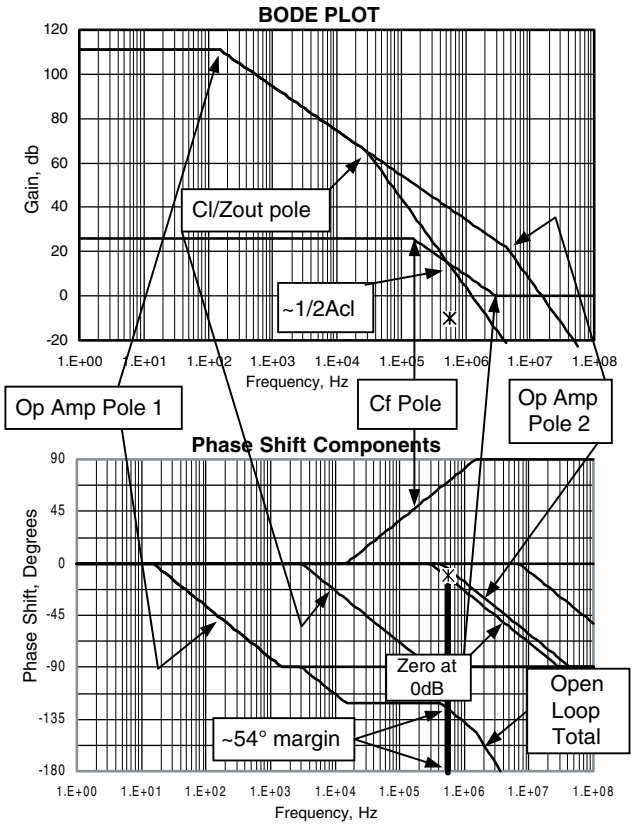


FIGURE 9. A CORRECTLY SIZED ROLL OFF CAPACITOR ACHIEVES STABILITY

our phase margin. In addition to careful layout, consider using lower values for the input and feedback resistors. Cutting the resistors in half will double the value of Cf, making errors due to parasitics less destructive.

Was this magic? No, just Power Design automation of Apex Application Note 25 on Driving Capacitive Loads. Refer to this and Application Note 19 on Stability for Power Operational Amplifiers for theory and formulas. You will learn that the closed loop phase shift curves we have been looking at are the sum of effects of all the poles and zeros in the circuit. The bottom curve of Figure 9 shows graphically most of the individual phase shift components. Individual phase shift relating to pole 1 is hidden under the total curve. The only positive going curve is the result of the pole of the roll off capacitor. Note the zero associated with Cf (-45° at 3MHz) when 1/beta reaches 0db. Do not fall into the trap of thinking that if a small capacitor is good, a bigger one must be better. This capacitor will certainly roll off signal amplitude below 0db, but it does not take 1/beta below 0db. A larger capacitor would produce a flat high frequency 1/beta at 0db, a high intersection rate and oscillation.

The roll off capacitor technique is very effective when closed loop gain is 20db or more. With a slope of 20db/decade on this segment, the frequency spacing of the pole and zero are directly related to closed loop gain. As gain decreases the pole and zero become closer together and cancel each other.

THE NOISE GAIN COMPENSATION NETWORK

The last technique requires two components and requires the non-inverting input to be hard grounded. The hardware is a series connected R-C from the summing junction to ground. The Power Design schematic has them labeled Rn and Cn. With this network grounded, it does not change gain of the signal path. At high frequencies, where you would think of Cn as appearing as a short, the noise of this circuit will increase because it has two input resistors in parallel making the net gain higher. The real objective, however, is to increase 1/beta or to reduce the fraction of the output signal fed back to the inverting input.

Please: Visualize, “feel” and refer to Figure 10 with a modified problem statement. The capacitive load is only 5nF this time, but this is enough to yield a phase margin of ~8°. Step one is to imagine a new horizontal line located 20db above the original closed loop gain. Note the frequency where the new line crosses the open loop gain curve. Step two is dividing by something between 3 and 10. For now, let’s pick 10 and hope your answer is somewhere in the area of 20KHz. ***This will be the pole location of the noise gain network.***

MODEL	PA85-100	Note/PBs	Rn	9999999999	Kohms
Rcl	3	Ohms	Cn	0	nF
Cload	0.005	uF	Cf	0	pF
Rin	10	Kohms	Riso	0	Ohms
Rf	190	Kohms			
Notes:					
R-C Pole Calculator:					
1	Kohms	2.5	Kohms	25	KHz
20	KHz	0.002	nF	0.005	uF
7.95775	nF	31830.989	KHz	1273.239545	Ohms

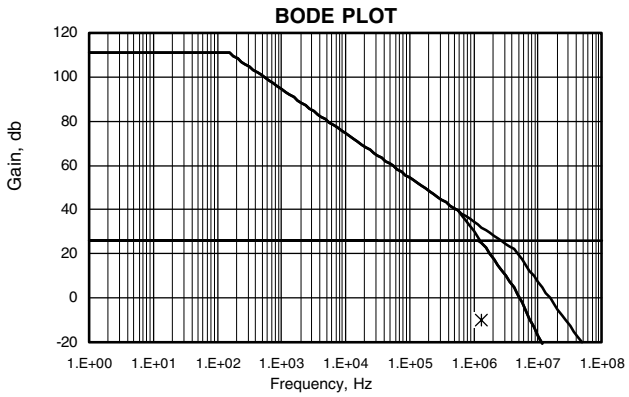


FIGURE 10. A NEW PROBLEM TO CONQUER

The 20db elevation of the new line segment is important; too little does not help enough, too much gets to be just as bad. Select the value of Rn such that when paralleled with Rin, the non-inverting gain goes up by a factor of 10. An approximation is simply Rin/10, which has already been entered in the R-C Pole Calculator. Power Design tells us this approximation yields 20.4db. Entering the desired pole frequency of 20KHz yields 8nF. We will use 8.2nF and proceed to Figure 11 (next page).

Noise gain compensation works best when the pole formed by output impedance and capacitive load is not more than 20db above the closed loop gain.

A COMBO DEAL IS NOT ALWAYS FAST FOOD

We found that a minimum closed loop gain of 20db is desirable for the roll off capacitor to do a good job. Also, for the noise gain compensation to produce good results, we want no more than 20db between closed loop gain and the pole produced by output impedance and the load capacitor. There are a fair number of applications requiring a signal gain of -1, which is a 1/beta of only 6db. See Figure 12 (next page) as our next problem statement. This circuit is an ideal candidate for a combination of both roll off capacitor and noise gain techniques.

As a first step, select Rn for a 20db increase of 1/beta or non-inverting gain (5K was used in this example). For a trial,

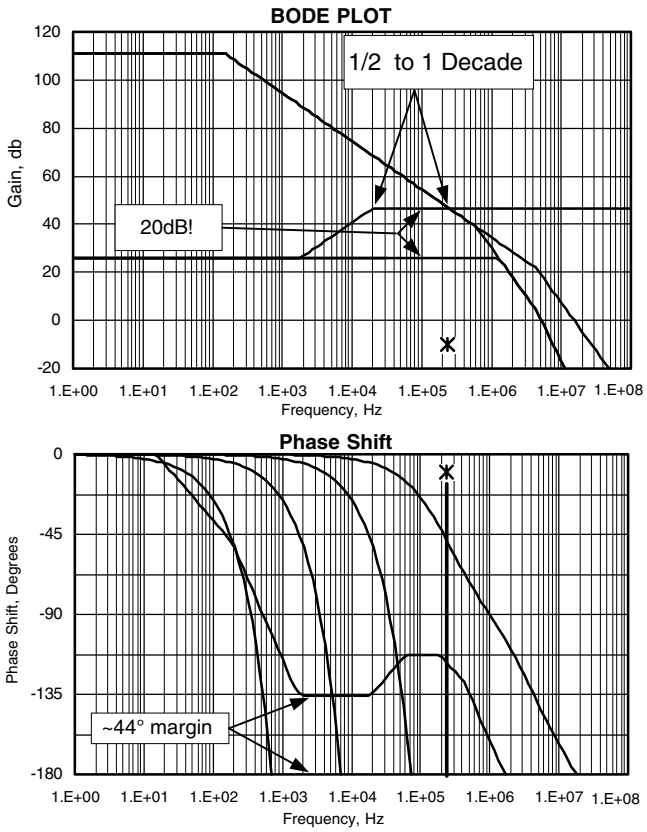


FIGURE 11. THE NOISE GAIN COMPENSATION NETWORK DOING ITS THING

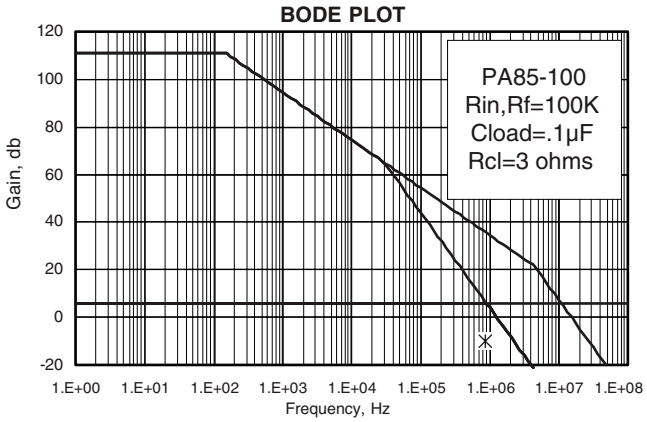


FIGURE 12. LOW GAIN AMPLIFIERS PRESENT THE BIGGEST CHALLENGE

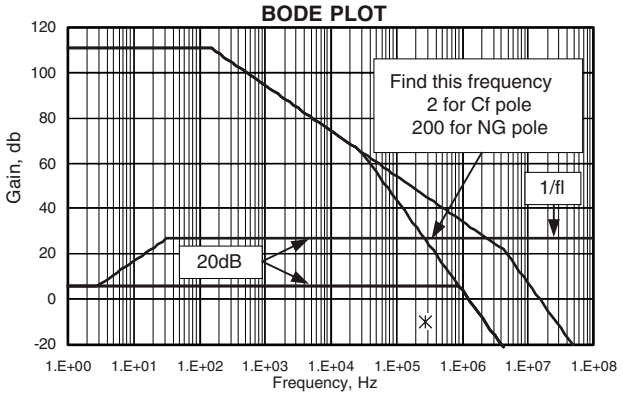


FIGURE 13. SETTING UP THE INITIAL NOISE GAIN CURVE

enter 1000nF for Cn and refer to Figure 13 showing our new 1/beta. Divide the frequency where 1/beta crosses open loop gain (~250KH) by 2 and set the Cf pole accordingly. Set the noise gain pole two decades lower yet. The R-C Pole Calculator makes it easy to select 12pF for Cf and 27nF for Cn. Figure 14 shows the results.

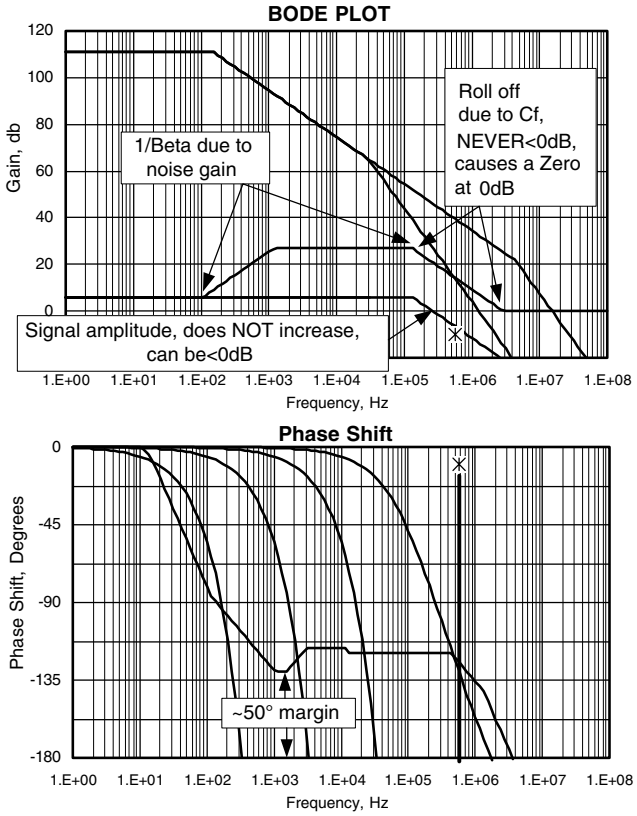


FIGURE 14. COMBINING NOISE GAIN WITH A ROLL OFF CAPACITOR

COMPARING THE METHODS

Your Daddy probably avoided using the isolation resistor technique because of the dreaded voltage drop outside the loop. But being of the enlightened age, you will look at the roll off error shown in Figure 15 and realize this error applies to any feedback capacitor inside the loop as well! This means that when pole frequencies are equal, gain errors introduced by either an isolation resistor or a feedback capacitor are identical.

We also need to look at the phase shift issue. The lower graph of Figure 15 (next page) shows the phase shift occurring outside the loop; an error to be added to the closed loop phase shift to find total phase shift applied to the actual load. Comparing the closed loop phase shift of Figure 7 (the isolation resistor solution) to that of Figure 9 (the feedback capacitor solution) reveals much better phase performance when the isolation resistor is used. The key to this difference is that adding the feedback capacitor introduces both a positive and a negative component to open loop phase shift while adding an isolation resistor introduces only a positive component. This difference can be seen directly in the Phase Components graphs. For an indirect indicator, notice that open loop phase beyond the closure frequency falls off more rapidly with the Cf solution than with the Riso solution. Table 1 shows gain errors and total phase shift errors for the two circuits at the suggested maximum bandwidth and several points below. With the pole frequency of the isolation resistor solution a little higher than the

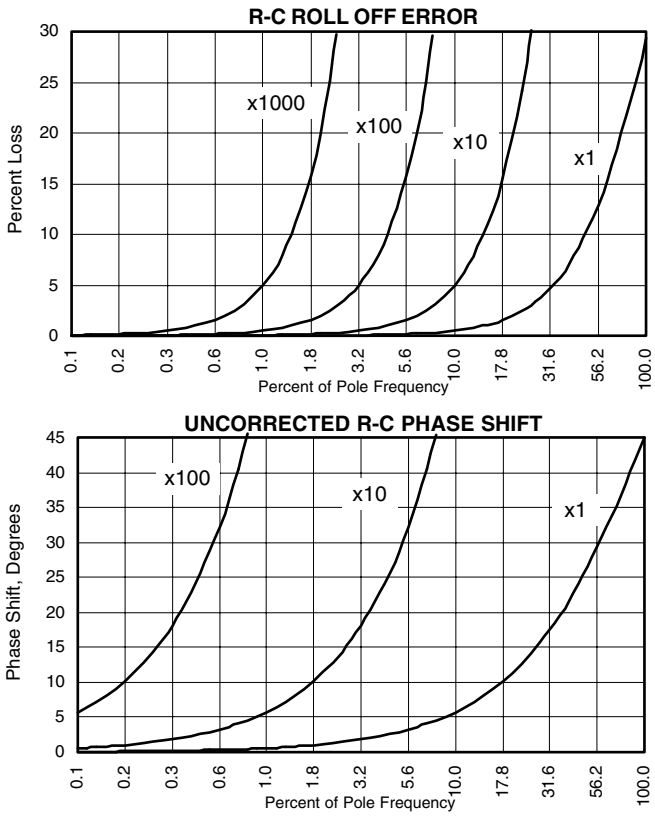


FIGURE 15. R-C ROLL OFF AMPLITUDE ERROR AND UNCORRECTED PHASE SHIFT

pole of the feedback capacitor solution, both gain and phase performance of the isolation resistor solution is superior.

	865KHz	43KHz	22KHz	8.6KHz	860HZ
Cf Gain	12.8%	4%	1.1%	0.17%	0.002%
Riso Gain	8.7%	2.4%	0.62%	0.1%	0.001%
Cf Phase	40	21	11	4.3	0.43
Riso Phase	37	19	9.5	3.9	0.39

TABLE 1. TOTAL GAIN AND PHASE ERRORS FOR Cf AND RISO SOLUTIONS

WORKING WITH COMPOSITE AMPLIFIERS

Stability headaches seem to escalate exponentially with the number of amplifiers in the loop, so most designers tend to avoid them. However, the composite is often worth the extra trouble when large power levels and high DC accuracy are both required. The techniques to achieve stability with the composite are basically the same as we already covered; stabilize the power stage first, then repeat the job for the total circuit.

Figure 16 is the data entry screen for the second half of this work. The first half is represented by the Pwr symbol (accomplished as above), and those numerical results become input data for this half. The schematic is showing that the closed loop response of the power stage is in series with the host amplifier, or is being added to the open loop response of the host amplifier. Stability analysis for the composite performs exactly that addition and a typical result and the classic problem with the composite is shown in Figure 17.

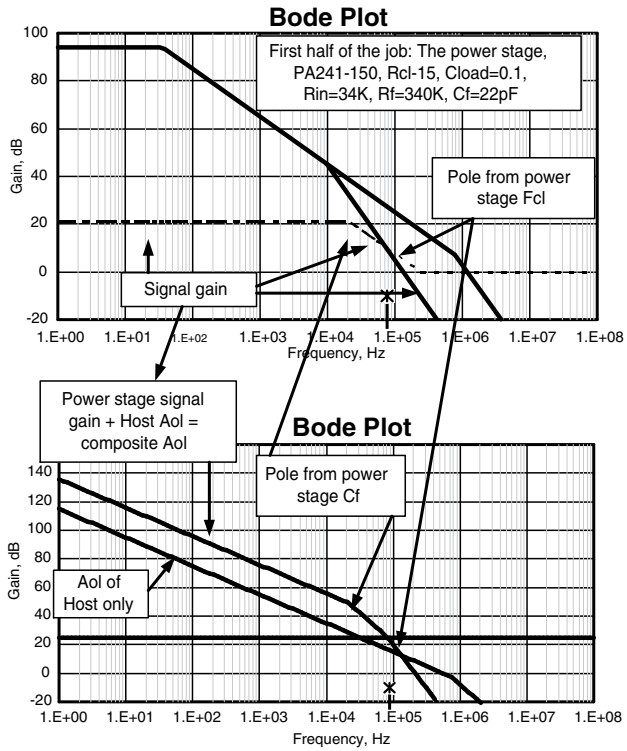


FIGURE 17. A POWER STAGE RESPONSE INCORPORATED INTO A COMPOSITE AMPLIFIER

The OP07 host amplifier has a well behaved open loop gain curve with its second pole near 0db gain. If the small signal amplifier you wish to use is not included in the built-in data base, Power Design comments tell how to enter data extracted from a data sheet. The model of the composite open loop gain features the poles of both the host amplifier and the closed loop power stage response. The pole at ~21KHz (due to the roll off capacitor in the power stage) causes an intersection rate of 40db/decade for any closed loop gain between 25db and 45db. Lower gains would yield 60db/decade because closure frequency in the power stage places pole just over 70KHz. It is quite possible to see this type stability problem even when not driving a capacitive load..

Power Design provides two techniques to stabilize the com-

Composite Circuits

MODEL	OP07	READ ME				Estimated Closure Frequency =	86.59643	KHz
Aol =	135	dB	Pole 1 =	0.1	Hz	Suggested maximum bandwidth	27.3842	KHz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06	Hz	Estimated Closure Rate =	60.0	dB/decade
Rin	21	Kohms	Rn	99999999999	Kohms	Estimated Phase Margin =	-35.95021	Degrees
Rf	340	Kohms	Cn	0	nF			
Cf	0	pF	Using Look-Up data					
Notes:								
R-C Pole Calculator :								
3.4	Kohms	47	Kohms					
5	KHz	10	nF					
9.36206	nF	0.338627538	KHz					
1/Beta (DC)		24.7	dB					
Noise Gain		0.0	dB					
Pole Noise Gain		0.015915494	KHz					
Zero Noise Gain		0.015915494	KHz					
Pole Cf/Rf		4681027738	KHz					
Zero Rf/Cf		80469095893	KHz					

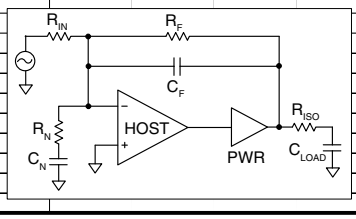


FIGURE 16. ENTERING HOST AMPLIFIER FOR THE COMPOSITE CIRCUIT

posite circuit. If an isolation resistor was used, it is modeled in the power stage only and its effects are included in the closed loop response data fed into the composite problem statement. You may use the roll off capacitor, the noise gain network or both as shown in Figure 18. The same basics on component selection apply here, but you may find a little more tweaking of component values is required. Final values for the solution shown are Rn=3.4K, Cn=10nF and Cf=22pF which yield a phase margin of 50°.

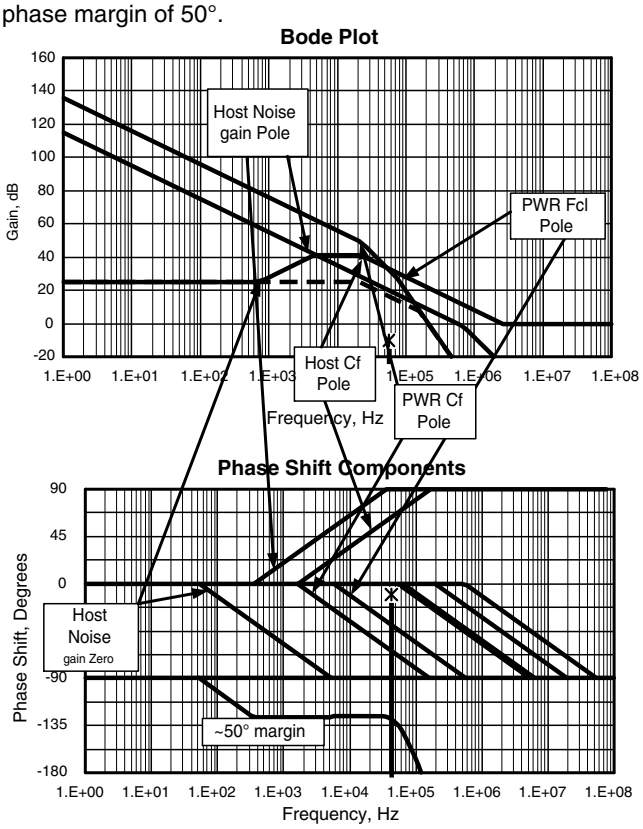


FIGURE 18. THE FINISHED COMPOSITE AMPLIFIER

DOES INDUCTANCE ALWAYS BRING STABILITY PROBLEMS?

The answer is no. You can drive inductance all day long in the voltage mode without waking the dragon. The problem is current mode drive where inductive V-to-I phase shift is inside the loop, courtesy of the current sense element. Figure 19 illustrates a combination of typical topologies on the data entry screen. We will address the numbered boxes later.

The most simple real topology is realized by applying the input signal to the non-inverting input and not using Rin. The power op amp drives the load in phase with the input signal to whatever amplitude is required to obtain voltage across Rs equal to the input signal. Adding Rin (grounded) to the circuit causes the voltage across Rs to be greater than the input signal.

To achieve an inverting circuit, ground the non-inverting pin and apply the signal to Rin. The op amp will drive the load out of phase at an amplitude large enough to develop a voltage on Rs equal to Rf/Rin. This inverting setup has dual advantages over the non-inverting circuit. Voltage on the sense resistor can be larger or smaller than the input signal, plus there is no common mode voltage on the amplifier.

Notice that in both circuits the load impedance is inside the feedback loop, meaning closed loop gain is partially a function of load impedance. This is exactly what we want for current control; load impedance goes up; gain goes up; output voltage goes up; and current remains constant. Refer to Figure 20 for a picture of the problem with “the gain goes up”. Open loop

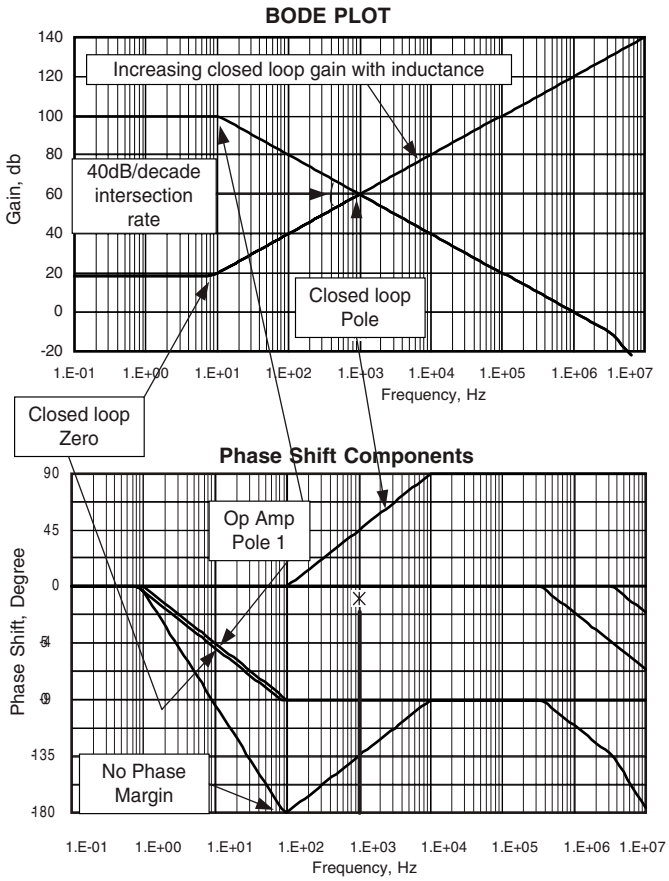


FIGURE 20. GAIN AND PHASE PROBLEMS CAUSED BY INDUCTANCE IN THE FEEDBACK LOOP

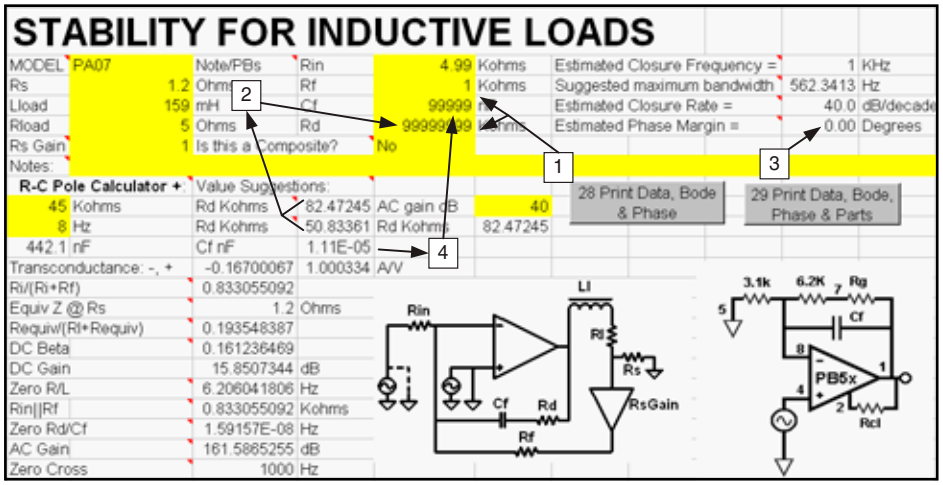


FIGURE 19. STEPS TO STABILITY FOR CURRENT CONTROL WITH INDUCTIVE LOADS

gain is falling at 20db/deacade and closed loop gain is rising at 20db/decade to produce an intersection rate of 40db/decade; an event of which we've grown suspicious.

When it comes to adding all the phase shift elements to find open loop phase shift (and phase margin), notice that the first pole in the open loop response of the op amp is nearly coincident with a zero in the closed loop. This causes open loop phase to drop like a rock to 180° (zero phase margin) at 100Hz. The key to stabilizing this circuit will be to lower the frequency of the closed loop pole (currently at the intersection point) by using a second feedback path consisting of Cf and Rd.

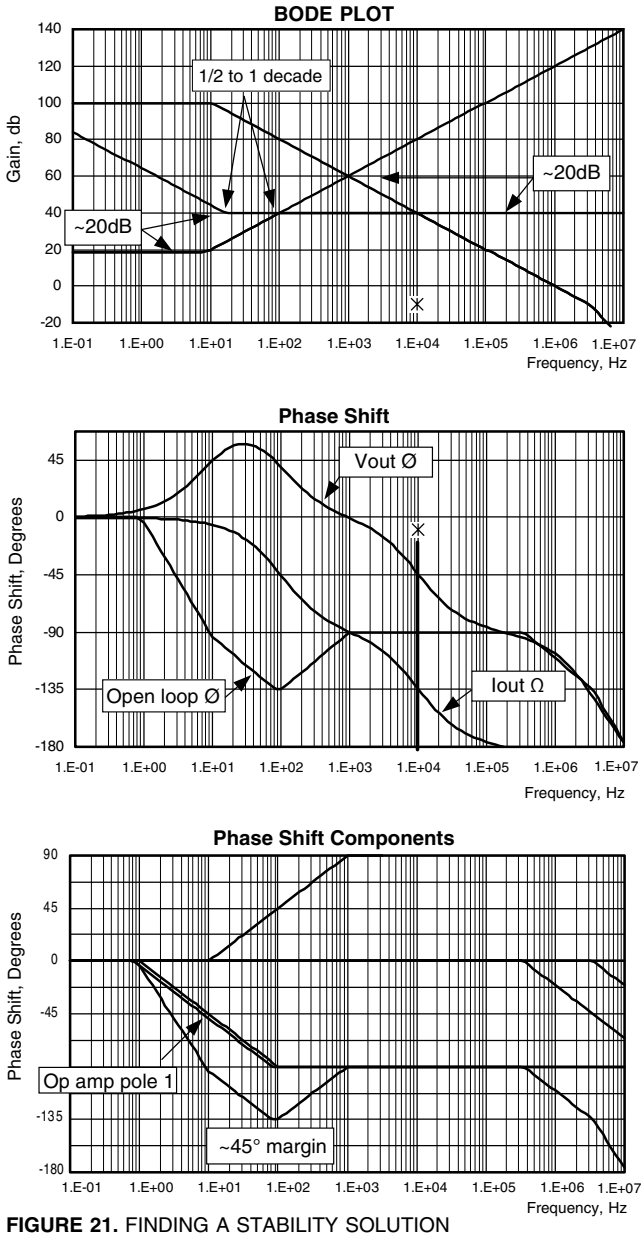


FIGURE 21. FINDING A STABILITY SOLUTION

This R-C network will introduce a second feedback path doing practically nothing at low frequencies but providing dominant voltage feedback at higher frequencies, without the additional V-to-I phase shift of the inductor. Figure 21 shows a typical solution where the flat portion of this feedback path is usually positioned at least 20db above DC gain or 20db below the intersection of open loop gain and the inductive feedback path. If there is a conflict between these to goals, start with the higher db level. The corner frequency of the R-C network is usually about 3/4 of a decade below the intersection of the two feedback paths.

The circuit function of our example is an inverting amplifier with an input signal of ±10V and a transfer function of 0.167A/V. At peak currents of 1.67A, power dissipation in the sense resistor seemed acceptable and values of Rin and Rf were convenient. Please note that these same component values could model a non-inverting amplifier with a transfer function of 1A/V.

Refer to Figure 19 again to see that Power Design calculates two values for Rd and then a value for Cf. To use these features:

1. Enter large values for both Cf and Rd.
2. Enter the larger recommendation for Rd.
3. If phase margin is well over 45°, raise Rd, if less, lower Rd.
4. When satisfied with phase margin, enter recommendation for Cf.

In this example, values of 82K ohms and 120nF were used.

As transfer functions and Q ratings of inductors change, the curves Power Design draws for you will vary a lot. As in this example, some will fall into place with suggested values; some will require playing with the value of Rd; and a few may require no network at all. When viewed as a single issue, stability for these amplifiers is simple. However, you will often find yourself fighting for bandwidth. The good news is that re-running the stability analysis for a dozen sets of gain and sense resistors is an easy task. As a general rule, large sense resistors and low gain settings will maximize bandwidth.

THEORY IS GREAT--------BUT

We have mentioned parasitics and layout concerns a couple of times. Please pull from your memory the old phrase, "too broad a subject to cover....". True, so we will get right to Figure 22 (next page) and say the job is positively not finished until the hardware is tested. Use all components as close to production version as possible; power supplies, cable harnesses, signal sources, loads and any thing else you can think of.

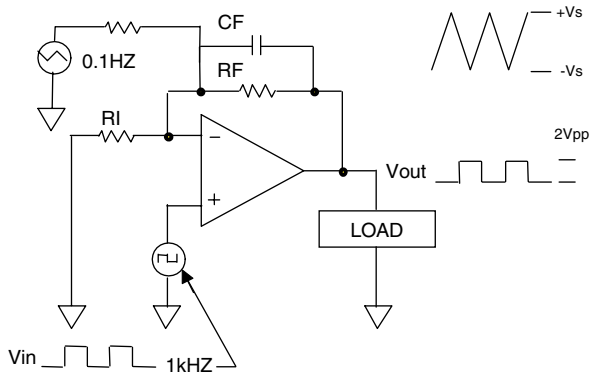
Watch the 1KHz output signal for over/under shoot while setting the very low frequency signal to exercise the amplifier output (plus the supplies, cables and the load) over the entire dynamic range. Then estimate phase margin of the system using the graph. A little time spent here now may keep you off the production line in six months.

CONCLUSION

The next time you happen to be involved in a nightlong argument about whether stability is a science or a black art, just smile. You won't have to say anything, just keep smiling. It would be good though, if you have your laptop along loaded with Power Design. When you think the smiling is about to get you smacked, tell the crowd both arguments are correct; arithmetic is the science portion, but expecting anyone to remember all the rules and formulas is the black art. With almost instant calculations and graphic data presentation, arithmetic is a snap and a lot of the rules can remain hidden. Power Design's built-in documentation presents the most important procedures and rules at the command of your mouse. The entire process becomes so easy, tasks like checking worst case component tolerances become bearable.

You'll be the hit of the party.

SQUARE WAVE TEST



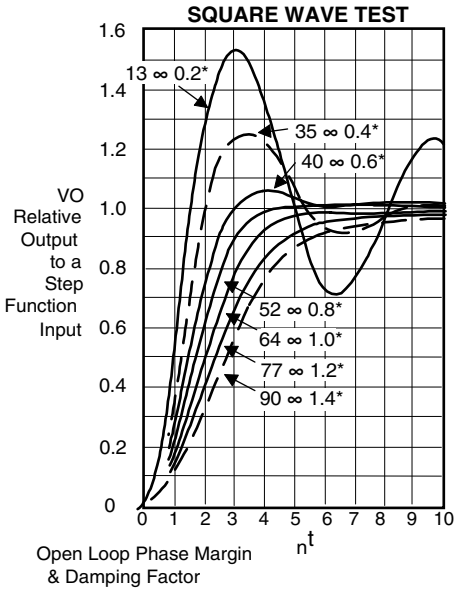


FIGURE 22. TESTING THE ENTIRE SYSTEM HARDWARE FOR PHASE MARGIN

